What is Claimed is:

[c1] A capacitor formed on a substrate, comprising:
a single-crystal Fin structure having a top surface and a first side surface opposite a second side surface;
an insulator structure adjacent the top surface of the at least one Fin structure; and
a conductor structure adjacent the at least one insulator structure over a portion of the at least one Fin structure.

[c2] The capacitor of claim 1, further comprising at least one first interconnect disposed adjacent one of the top surface, the first side surface, and the second side surface of the at least one Fin structure.

[c3] The capacitor of claim 1, further comprising at least one second interconnect disposed adjacent the at least one conductor structure.

[c4] The capacitor of claim 1, wherein the at least one conductor structure is selected from the group consisting of a metal, a metal silicide, and doped polysilicon.

[c5] The capacitor of claim 1, wherein the at least one single-crystal Fin structure has a given width, and wherein the at least one conductor structure partially at least one Fin structure.

[c6] The capacitor of claim 1, wherein the at least one single-crystal Fin structure is narrow, has a given width and wherein the at least one insulator structure is adjacent both the first side surface and the second side surface of the at least one Fin structure, thereby encapsulating the at least one Fin structure.

[c7] The capacitor of claim 6, wherein said first single-crystal Fin structure has conductivity-enhancing dopant ions therein.

[c8] The capacitor of claim 1, wherein a FinFET is disposed on the substrate, the FinFET having a gate electrode coupled to said conductor structure.

[c9] The capacitor of claim 9, wherein the substrate comprises a SOI substrate.

[c10] An integrated circuit chip comprising at least one first nominal-voltage decoupling capacitor and at least one second high-voltage decoupling capacitor, respectively comprising:

a first single-crystal Fin structure having a first width and second single-crystal Fin structure having a second width greater than said first width, each having a top surface and a first side surface opposite a second side surface;

a first insulator structure adjacent the top surface, the first side surface, and the second side surface of the first Fin structure, thereby encapsulating the first Fin structure, and at least one second insulator structure adjacent the top surface of the second Fin structure; and

a first conductor structure adjacent the first insulator structure over a portion of the first Fin structure, and second conductor structure adjacent the at least one second insulator structure over a portion of the second Fin structure so that the second conductor structure partially overlays is within a thickness of the second Fin structure.

[c11] The integrated circuit chip of claim 10, wherein said second single-crystal Fin structure has conductivity-enhancing dopant ions therein.

[c12] The integrated circuit chip of claim 10, wherein first conductor structure substantially overlies said first Fin structure, and said second conductor structure only partially overlies said second Fin structure.

[c13] A method of forming at least one capacitor, the method comprising the steps of:

forming a plurality of single-crystal Fin structures having a top surface and a first side surface opposite a second side surface;

forming insulator structures adjacent all of said surfaces of each of said plurality of one Fin structure; and

forming conductor structures adjacent at least a portion of said insulator structures of each of said Fin structures.

[c14] The method of claim 13, wherein said step of forming said plurality of single-crystal Fin structures comprises the steps of:

forming a patterned hardmask on a semiconductor layer disposed ona substrate; and

etching said semiconductor layer by exposure to a anisotropic etchant.

[c15] The method of claim 14, wherein said step of forming said patterned hardmask comprises the steps of

forming a mandrel structure on said semiconductor layer, said mandrel structure having

first and second sides;

forming sidewall spacers on said first and second sides of said mandrel structure; and

removing said mandrel structure without substantially removing said sidewall spacers.

[c16] The method of claim 14, further comprising doping the Fin structure said etching step with a suitable dopant.

[c17] The method of claim 14, wherein said sidewall spacers are used to etch said semiconductor layer in areas where a Fin structure of a first width are to be formed, and wherein said sidewall spacers are not used to etch said semiconductor layer in areas where a Fin structure of a second width greater than said first width are to be formed.

[c18] The method of claim 17, wherein said Fin structures of said first width is used to form capacitors and FETs, respectively, and said Fin structures of said second width are used to form capacitors.

[c19] The method of claim 17, wherein said conductor structures substantially overlay the Fin structures of said first width and only partially overlay the Fin structures of said second width.